Randev Ranjit

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MSc Computer & Embedded Systems Engineering, TU Delft • graduating 2028, available full-time from graduation

Delft, NL • github.com/RandevRanjit • randevranjit.github.io/portfolio • LinkedIn

Digital Design & FPGA

Cellular-Automaton Accelerator for a RISC-V SoC • *SystemVerilog, Questa, Vivado, Artix-7* **2025 – 2026**

System-on-Chip Design coursework (individual); driven from RISC-V over MMIO and demonstrated live on the board

- Designed the drawing unit from scratch: programmable Wolfram rule, 32-bit LFSR seed, 3-state FSM, byte-enabled framestore writes over req/ack. Under back-pressure the FSM holds address, data and byte-enables until ack.
- Verified with **SVA** on the req/ack handshake and a stall-injection shim forcing back-pressure; forced a reset mid-run to reach the last FSM transition. **100 % statement, branch, condition and FSM coverage** in Questa.
- Wrote an 874-line self-checking testbench (framestore model, 502-pixel golden image, 7 SVA properties) that flagged **4 of 5** supplied drawing units as faulty: no ack, ack held past one cycle, every write lost, sloped lines missing.
- **Placed and routed on Artix-7**: block used 4,433 LUTs, 1,467 FFs, 0 BRAM, 1 DSP; SoC BRAM-bound at 96 % by the supplied framebuffer. Traced the one DSP to the $y \cdot (W/4)$ row-address multiply.

Stump 16-bit RISC CPU • *Processor Microarchitecture coursework; Verilog, ModelSim, ISE, Spartan-6* **2024**

- Multi-cycle CPU (board wrapper and memory model supplied): datapath, 8-function ALU, shifter, 8-register file, 3-state control FSM (fetch, execute, memory), load/store and branch paths; self-checking testbenches.
- Placed and routed on Spartan-6 at 2,068/2,400 LUTs and 591/600 slices (98 %); wrote Battleship in Stump assembly.

Education

Delft University of Technology • MSc Computer & Embedded Systems Engineering **Sep 2026 – 2028**

Current modules: Hardware Fundamentals; Digital Computing Systems; Systems Engineering. Computer Architecture specialisation planned; summer 2027 internship creditable to the MSc (CESE5010, 15 EC).

University of Manchester • BSc (Hons) Computer Science, Upper Second (2:1) **Sep 2022 – Jul 2026**

Hardware modules: System-on-Chip Design; Processor Microarchitecture; Chip Multiprocessors; System Architecture.

UWC South East Asia, Singapore • International Baccalaureate, 39/45 **2022**

Experience

Manchester Stinger Motorsport (Formula Student) • AI Lead (Simulation & Control) **2022 – 2026**

- Led the **10–15 person** driverless (FS-AI) sub-team for three years and wrote about **29k of the 34k lines** of its C++20 simulator. Set technical direction and coordinated integration and testing with the wider 300-member team.
- Sole author of the autonomy-to-VCU CAN layer (3.6k lines of C++, public): bit-level codec for 14 ADS-DV messages over SocketCAN, a packed 13-byte CAN-over-UDP frame, message-rate and watchdog tests on a simulated VCU.

CarrLane Manufacturing, Chennai, India • AI / Software Engineering Intern **Jun – Aug 2025**

- Built an LLM function-calling assistant (9 typed tool schemas, FastAPI + SQLite) for natural-language part lookup.

Real-Time & Parallel Software

Final-year dissertation: reactive controller (RRHC) vs MPCC • *Python, CasADi/IPOPT* **2025 – 2026**

- Per-step latency audit at 50 Hz (20 ms deadline): RRHC P99 0.16 ms with no misses. The MPCC averaged 19.9 ms, but its P99 was 115 ms and it missed the deadline **1,870** times in three laps.
- Same plant, course and control rate for both: RRHC lapped 12.2 % faster at 1/153 of the compute, and was faster in 22/22 paired conditions (Wilcoxon $p = 1.9 \times 10^{-5}$).

Chip Multiprocessors labs • *C, C++20, pthreads, OpenMP, 72-core two-socket Xeon* **2026**

- Fixed four synchronisation bugs in a supplied stencil (no barrier, per-thread swap, per-thread exit, clobbered iteration count), then added temporal blocking: **132**× over serial on 72 threads (95 % lower bound 124×).
- NUMA-aware vector add at 30.7× on 72 threads (bandwidth-bound). Fine-grained spinlocks took dining-philosophers throughput from a coarse-lock plateau of about 123k to 1.04M meals/s at 64 threads.

Skills

HDL & EDA: SystemVerilog, Verilog; RTL/FSM design; Questa/ModelSim (SVA, code coverage); Vivado, Xilinx ISE
Interfaces & systems: CAN (SocketCAN), UDP sockets, UART, memory-mapped I/O; pthreads, OpenMP, NUMA
Languages & tools: C, C++20, Python, RISC-V assembly; Git, CMake, Linux, Eigen, OpenGL

Additional

Right to work (NL): credited internship needs no permit; orientation-year permit from graduation.